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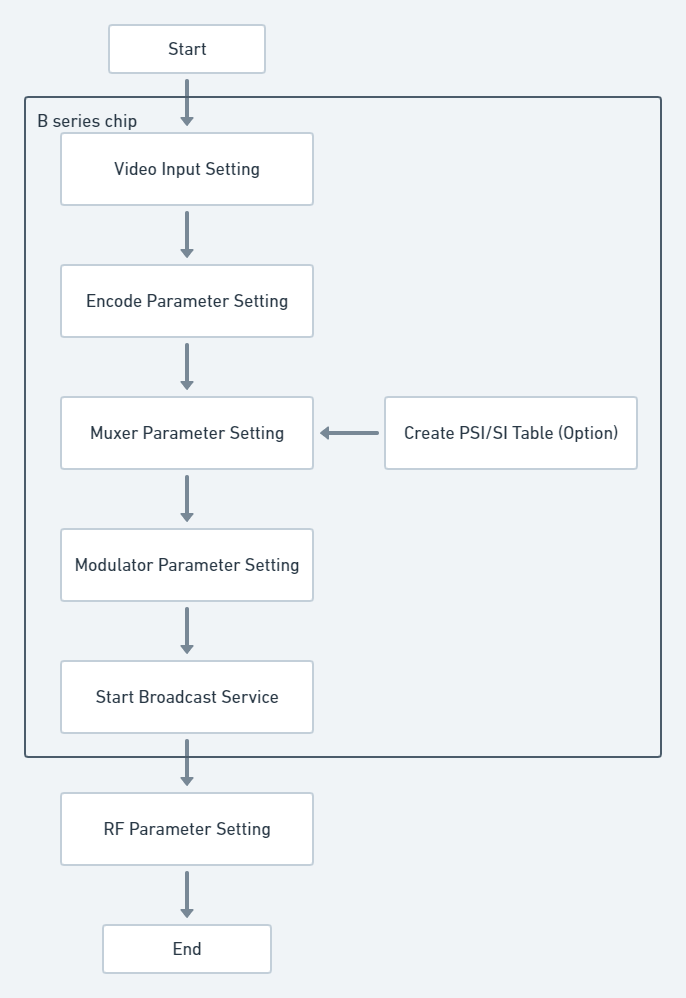
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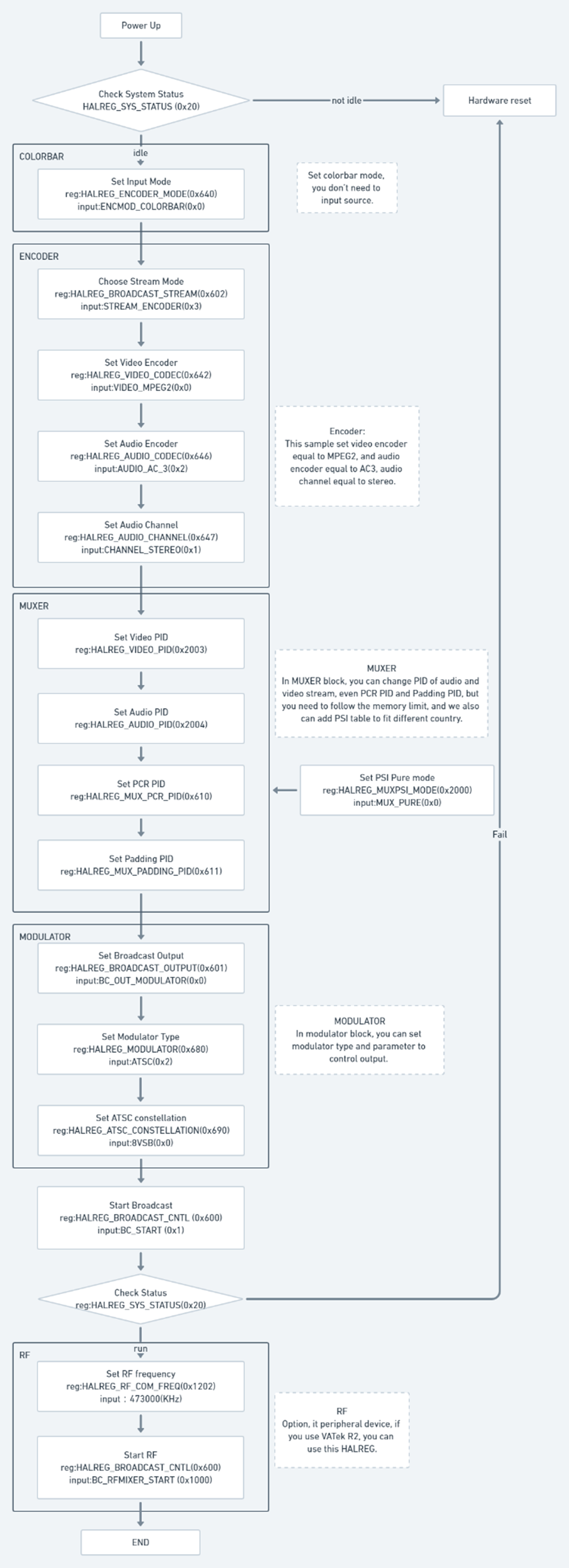
## 1. System Process

### 1.1 Process Overview

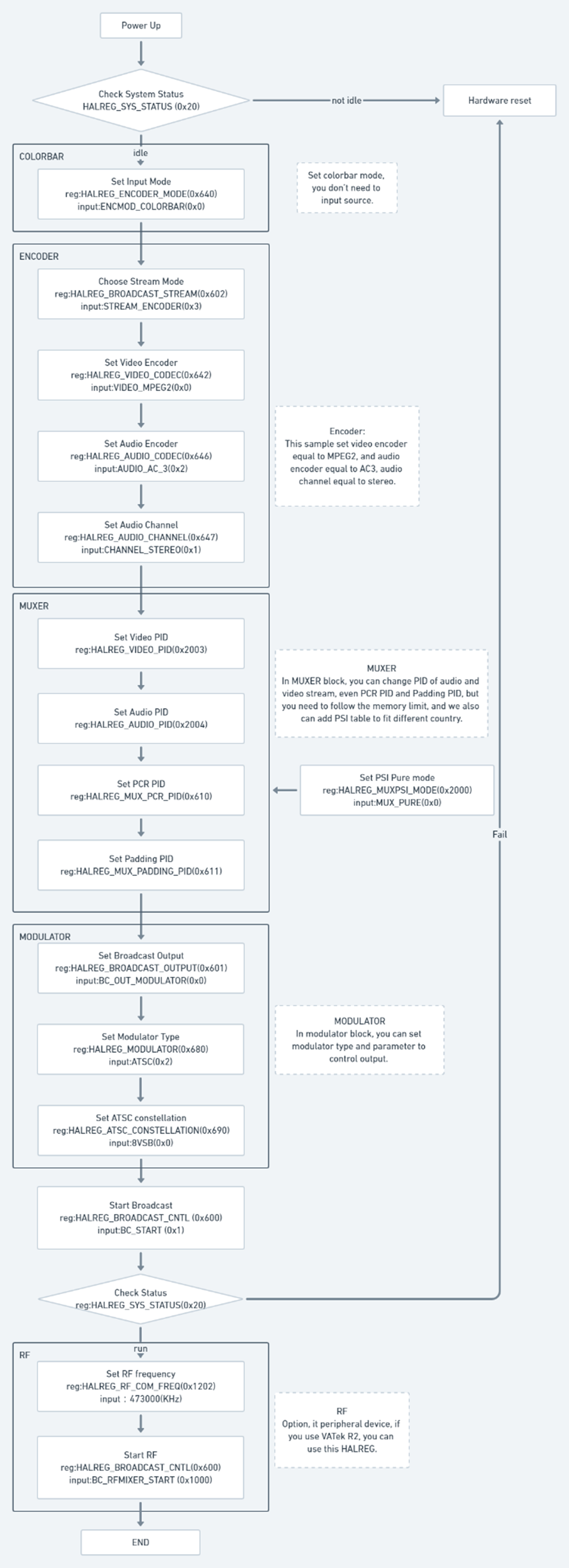


### 1.2 Process of chip (color bar)

You can use color bar as input source without input extra source.

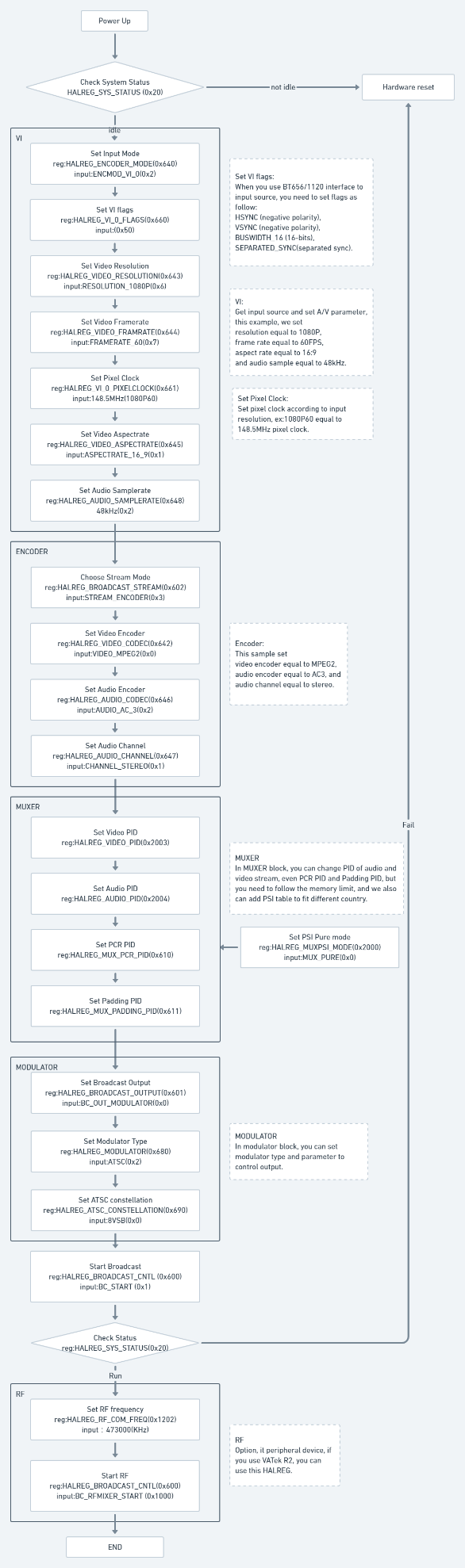


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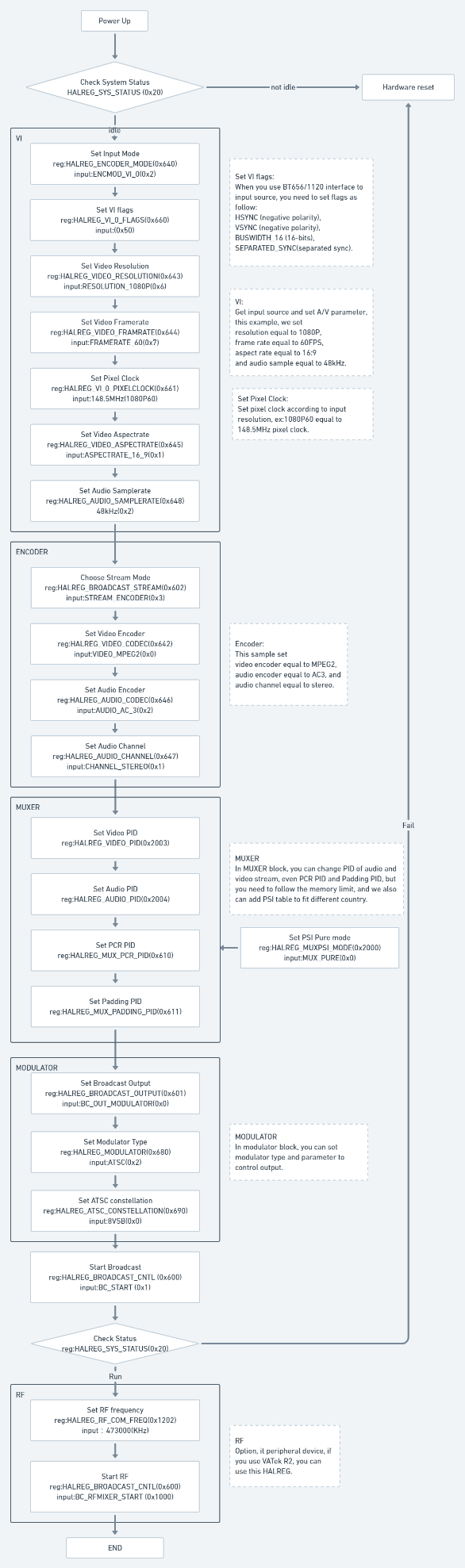


### 1.3 Process of chip (VI)

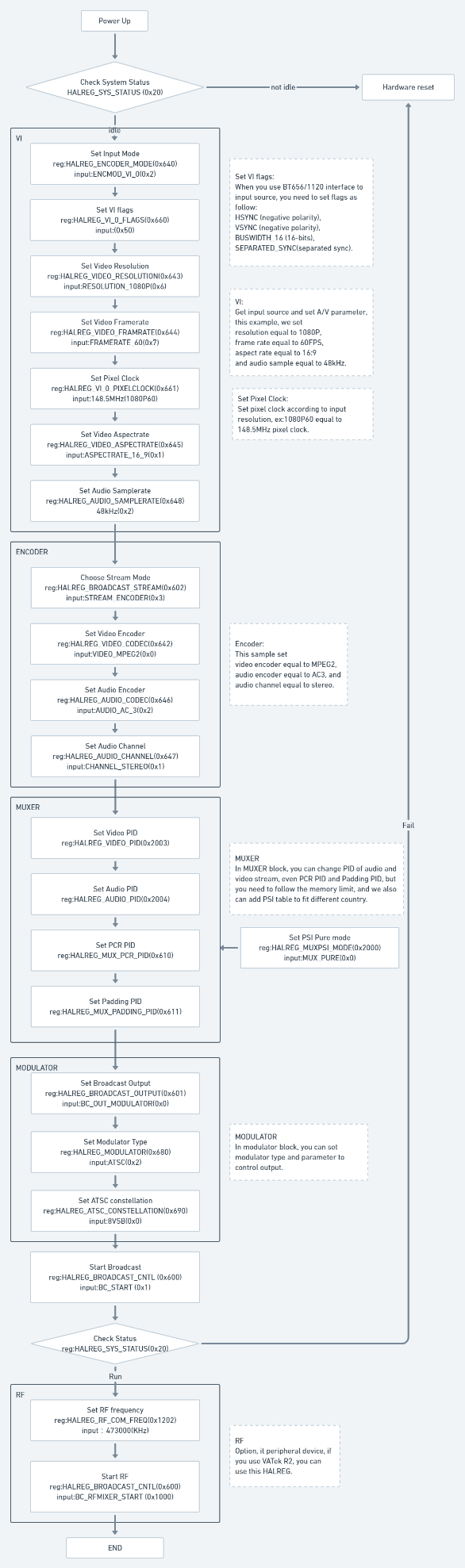
To using VI mode, you need to finish setting input PHY at the front end.



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## **2. Status Registers (BASE)**

### 2.1 System Status

**0x20 - HALREG\_SYS\_STATUS\_0:** System Status Register 0

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R | 0xFF000001 | SYS\_STATUS\_IDLE: |
| R | 0xFF000002 | SYS\_STATUS\_RUN: |
| R | 0xFF000085 | SYS\_STATUS\_LOADER\_FAIL |
| R | 0xFF000086 | SYS\_STATUS\_SERVICE\_FAIL |
| R | 0xFF000088 | SYS\_STATUS\_EXCEPTION\_FAIL |
| R | 0xFF00008E | SYS\_STATUS\_BADSTATUS |
| R | 0xFF00008F | SYS\_STATUS\_UNKNOWN\_FAIL |

**0x23 - HALREG\_SYS\_ERRCODE:** System Error Code Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R | 0x80000001 | SYS\_ERRCODE\_INIT |
| R | 0x80010001 | LOADER\_ERRCODE\_NOAPP |
| R | 0x80010002 | LOADER\_ERRCODE\_CRC32 |
| R | 0x80010003 | LOADER\_ERRCODE\_HW |
| R | 0x80020001 | SERVICE\_INIT\_FAIL |

**0x24 - HALREG\_CHIP\_ID:** CHIP ID Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R | 0x00010100 | HAL\_CHIPID\_A1 |
| R | 0x00010300 | HAL\_CHIPID\_A3 |
| R | 0x00020100 | HAL\_CHIPID\_B1 |
| R | 0x00020200 | HAL\_CHIPID\_B2 |
| R | 0x00020201 | HAL\_CHIPID\_B2\_PLUS |
| R | 0x00020300 | HAL\_CHIPID\_B3 |
| R | 0x00020301 | HAL\_CHIPID\_B3\_PLUS |

**0x25 - HALREG\_FW\_VER:** Firmware Version Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

**0x26 - HALREG\_SERVICE\_MODE:** Service Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R | 0xFF000001 | SERVICE\_TAG\_RESCUE |
| R | 0xF8000001 | SERVICE\_TAG\_BROADCAST |
| R | 0xF8000002 | SERVICE\_TAG\_TRANSFORM |

**0x27 - HALREG\_PERIPHERAL\_EN:** Peripheral Switch Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 |  | Reserved |  |
| 1 | R | 0x00000002 | PERIPHERAL\_FINTEKR2 |
| 2~15 |  | Reserved |  |
| 16 | R | 0x00010000 | PERIPHERAL\_EP9555E |
| 17 | R | 0x00000100 | PERIPHERAL\_USBBULK |
| 18 | R | 0x00000200 | PERIPHERAL\_AUXSTREAM\_USB |
| 19 | R | 0x00000400 | PERIPHERAL\_AUXSTREAM\_FLASH |
| 20 | R | 0x00000800 | PERIPHERAL\_AUXSTREAM\_TSIN |
| 21 | R | 0x01000000 | PERIPHERAL\_CALIBRATION |
| 22 | R | 0x70000000 | PERIPHERAL\_HWID\_MASK |
| 23~31 |  | Reserved |  |

**0x28 - HALREG\_INPUT\_SUPPORT:** Media Source Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | R | 0x00000001 | INPUT\_EN\_TEST |
| 1 | R | 0x00000002 | INPUT\_EN\_USB |
| 2 | R | 0x00000004 | INPUT\_EN\_TS |
| 3 | R | 0x00000008 | INPUT\_EN\_ENC |
| 4 | R | 0x00000010 | VENC\_EN\_MPEG2 |
| 5 | R | 0x00000020 | VENC\_EN\_H264 |
| 7 |  | Reserved |  |
| 8 | R | 0x00000100 | VENC\_EN\_FULLHD |
| 9~11 |  | Reserved | -- |
| 12 | R | 0x00001000 | AENC\_EN\_MP1\_L2 |
| 13 | R | 0x00002000 | AENC\_EN\_AAC\_LC\_ADTS |
| 14 | R | 0x00004000 | AENC\_EN\_AC\_3 |
| 15 | R | 0x00008000 | AENC\_EN\_AAC\_LC\_LATM |
| 20 | R | 0x00100000 | TEST\_EN\_HW |
| 21 | R | 0x00200000 | TEST\_EN\_REMUX |
| 22~31 |  | Reserved |  |

**0x29 - HALREG\_OUTPUT\_SUPPORT:** Output Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | R | 0x00000001 | OUTPUT\_EN\_MOD |
| 1 | R | 0x00000002 | OUTPUT\_EN\_SINEWAVE |
| 2 | R | 0x00000004 | OUTPUT\_EN\_TS |
| 3 | R | 0x00000008 | OUTPUT\_EN\_USB |
| 5~7 |  | Reserved |  |
| 8 | R | 0x00000100 | MOD\_EN\_DVB\_T |
| 9 | R | 0x00000200 | MOD\_EN\_J83\_A |
| 10 | R | 0x00000400 | MOD\_EN\_ATSC |
| 11 | R | 0x00000800 | MOD\_EN\_J83\_B |
| 12 | R | 0x00001000 | MOD\_EN\_DTMB |
| 13 | R | 0x00002000 | MOD\_EN\_ISDB\_T |
| 14 | R | 0x00004000 | MOD\_EN\_J83\_C |
| 15 | R | 0x00008000 | MOD\_EN\_DVB\_T2 |
| 16 | R | 0x00005F00 | MOD\_EN\_BASE |
| 17~31 |  | Reserved |  |

### 2.2 Broadcast Status

**0x620 - HALREG\_BCINFO\_STREAM:** Enable stream mode

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 3~31 | W | Reserved |  |

**0x621 - HALREG\_BCINFO\_OUTPUT:** Enable output mode

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 1~31 | W | Reserved |  |

**0x622 - HALREG\_BCINFO\_MODRATE:** Show output bitrate of MODULATOR.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

**0x623 - HALREG\_BCINFO\_MUXRATE:** Show output bitrate of MUX

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

**0x624 - HALREG\_BCINFO\_STATUS:** Broadcast Status Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | R | 0x00000000 | BCSTATUS\_IDLE |
| R | 0x00000001 | BCSTATUS\_WAIT\_SOURCE |
| R | 0x00000002 | BCSTATUS\_BROADCAST |
| R | 0x00000003 | BCSTATUS\_FINISH |
| 2~31 |  | Reserved |  |
| 32 | R | 0x80000000 | BCSTATUS\_FAIL\_UNKNOWN |
| R | 0x80000001 | BCSTATUS\_FAIL\_SOURCE |
| R | 0x80000002 | BCSTATUS\_FAIL\_TIMEOUT |
| R | 0x80000003 | BCSTATUS\_FAIL\_CODECDROP |
| R | 0x80000004 | BCSTATUS\_FAIL\_BUFFER |
| R | 0x80000005 | BCSTATUS\_FAIL\_MUXER |
| R | 0x80000006 | BCSTATUS\_FAIL\_ENCODE |
| R | 0x80000007 | BCSTATUS\_FAIL\_MEDIA |
| R | 0x80000008 | BCSTATUS\_FAIL\_DEMUX |

**0x625 - HALREG\_BCINFO\_CURRATE:** Show real bitrate of MUX

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

**0x626 - HALREG\_BCINFO\_DATARATE:** Show PES bitrate.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

**0x627 - HALREG\_BCINFO\_QUERYBUF:** Show buffer length.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

## 3.AV Control Registers (Stream Registers)

### 3.1 Registers for Video Input Settings

**0x643 - HALREG\_VIDEO\_RESOLUTION:** Video Encoder resolution

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | RESOLUTION\_480I |
| W | 0x00000001 | RESOLUTION\_480P |
| W | 0x00000002 | RESOLUTION\_576I |
| W | 0x00000003 | RESOLUTION\_576P |
| W | 0x00000004 | RESOLUTION\_720P |
| W | 0x00000005 | RESOLUTION\_1080I |
| W | 0x00000006 | RESOLUTION\_1080P |
| 3~31 |  | Reserved |  |

**0x644 - HALREG\_VIDEO\_FRAMERATE:** Video Encoder framerate

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | FRAMERATE\_23\_97 |
| W | 0x00000001 | FRAMERATE\_24 |
| W | 0x00000002 | FRAMERATE\_25 |
| W | 0x00000003 | FRAMERATE\_29\_97 |
| W | 0x00000004 | FRAMERATE\_30 |
| W | 0x00000005 | FRAMERATE\_50 |
| W | 0x00000006 | FRAMERATE\_59\_94 |
| W | 0x00000007 | FRAMERATE\_60 |
| 3~31 |  | Reserved |  |

**0x645 - HALREG\_VIDEO\_ASPECTRATE:** Video Encoder aspect rate

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | ASPECTRATE\_4\_3 |
| W | 0x00000001 | ASPECTRATE\_16\_9 |
| 1~31 |  | Reserved |  |

**0x647 - HALREG\_AUDIO\_CHANNEL:** Audio Encode Mode Select Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | CHANNEL\_MUTE |
| W | 0x00000001 | CHANNEL\_STEREO |
| W | 0x00000002 | CHANNEL\_MONO\_L |
| W | 0x00000003 | CHANNEL\_MONO\_R |
| W | 0x00000004 | CHANNEL\_STEREO\_MONO\_L |
| W | 0x00000005 | CHANNEL\_STEREO\_MONO\_R |
| 3~31 |  | Reserved | -- |

**0x648 - HALREG\_AUDIO\_SAMPLERATE:** Audio Sample Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | SAMPLERATE\_32KHZ |
| W | 0x00000001 | SAMPLERATE\_44\_1KHZ |
| W | 0x00000002 | SAMPLERATE\_48KHZ |
| 3~31 |  | Reserved |  |

**0x660 - HALREG\_VI\_0\_FLAGS:** Video Interface Setup Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~3 |  | Reserved |  |
| 4 | W | 0x00000010 | VI\_BUSWIDTH\_16 |
| 5 |  | Reserved | -- |
| 6 | W | 0x00000040 | VI\_SEPARATED\_SYNC |
| 7~8 |  | Reserved | -- |
| 9 | W | 0x00000200 | VI\_CLK\_INVERSE |
| 10 | W | 0x00000400 | VI\_HSYNC\_INVERSE |
| 11 |  | Reserved | -- |
| 12 | W | 0x00001000 | VI\_VSYNC\_INVERSE |
| 13~23 |  | Reserved | -- |
| 24 | W | 0x01000000 | VI\_FIELDID\_SIGNAL |
| 25~27 |  | Reserved |  |
| 28 | W | 0x10000000 | VI\_EXT\_HALF\_FPS |
| 29 | W | 0x20000000 | VI\_FIELD\_INVERSE |

**Description**

* VI\_BUSWIDTH\_16: setting output base on PHY, default is 0. 0 is 8-bits data; 1 is 16-bits data.
* VI\_SEPARATED\_SYNC: setting output base on PHY, default is 0。0 is Embedded Sync; 1 is Separated Sync.
* VI\_CLK\_INVERSE: setting output base on PHY, default is 0. 0 is trigger at rising edge; 1 is trigger at falling edge.
* VI\_HSYNC\_INVERSE: setting output base on PHY, default is 0. 0 is Negative Polarity; 1 is Positive Polarity.
* VI\_VSYNC\_INVERSE: setting output base on PHY, default is 0. 0 is Negative Polarity; 1 is Positive Polarity。
* VI\_FIELDID\_SIGNAL: setting output base on PHY, default is 0. 0 is using Field ID pin; 1 is detecting Field ID from timing.
* VI\_EXT\_HALF\_FPS: minus half frame rate from input. 0 is disable; 1 is enable.
* VI\_FIELD\_INVERSE: setting output base on PHY, default is 0. 0 is top field first; 1 is bottom field first.

**0x661 - HALREG\_VI\_0\_PIXELCLOCK:** Video Input Pixel Clock Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

### 3.2 Registers for AV Encoder Settings

**0x602 - HALREG\_BROADCAST\_STREAM:** Setting stream mode

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000003 | STREAM\_ENCODER |
| 1 | W | 0x00001000 | STREAM\_SINE |
| 2 | W | 0x00001001 | STREAM\_TEST |
| 2~31 |  | Reserved | -- |

**0x640 - HALREG\_ENCODER\_MODE:** Encoder Mode Control Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | ENCMOD\_COLORBAR |
| 1 | W | 0x00000001 | ENCMOD\_BOOTLOGO |
| 2 | W | 0x00000002 | ENCMOD\_VI\_0 |
| 3~31 |  | Reserved | -- |

**Description**

* ENCMOD\_COLORBAR: use SMPTE COLORBAR to be the output.
* ENCMOD\_BOOTLOGO: use boot logo to be the output which already store in v2img firmware file by user.
* ENCMOD\_VI\_0: use real input source from HDMI or CVBS interface

**0x641 - HALREG\_ENCODER\_FLAGS:** Encoder Mode Switch Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 |  | Reserved |  |
| 1 | W | 0x00000001 | ENC\_EN\_DISABLE\_DEINTERLACED |
| 2 | W | 0x00000004 | ENC\_EN\_PROGRESSIVE\_2\_I |
| 3 | W | 0x00000008 | ENC\_EN\_DISABLE\_ADTS\_CRC |
| 4 | W | 0x00000100 | ENC\_DIS\_LATENCY\_Q |
| 4~31 |  | Reserved | -- |

**Description**

* ENC\_EN\_DISABLE\_DEINTERLACED: specific function in chip of B3+ combine H1 HDMI PHY, if user want to input interlaced format and don’t need to change format, user can enable this function.
* ENC\_EN\_PROGRESSIVE\_2\_I: change progressive format to interlaced format and output interlaced format, 0 is disable, 1 is enable.
* ENC\_EN\_DISABLE\_ADTS\_CRC: in ADTS audio encoder, it needs to check, use this flag will skip the check and output audio information, 0 is disable, 1 is enable.
* ENC\_DIS\_LATENCY\_Q: user can remove relation of latency and quantity by enable this flag.

**0x642 - HALREG\_VIDEO\_CODEC:** Encoder format

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | VIDEO\_MPEG2 |
| W | 0x00000001 | VIDEO\_H264 |
| 2~31 |  | Reserved |  |

**0x646 - HALREG\_AUDIO\_CODEC:** Audio Encoder format

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | AUDIO\_MP1\_L2 |
| W | 0x00000001 | AUDIO\_AAC\_LC\_ADTS |
| W | 0x00000002 | AUDIO\_AC\_3 |
| W | 0x00000003 | AUDIO\_AAC\_LC\_LATM |
| 2~31 |  | Reserved |  |

**0x2002 - HALREG\_ENCODER\_PMTPID:** set PMT PID in default mode.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x2003 - HALREG\_VIDEO\_PID:** set PID of video PES

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x2004 - HALREG\_AUDIO\_PID:** set PID of audio PES

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

## 4. MUXER register

### 4.1 Mux Related Settings

**0x610 - HALREG\_MUX\_PCR\_PID:** set PID of PCR

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x611 - HALREG\_MUX\_PADDING\_PID:** set PID of padding buffer

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x612 - HALREG\_MUX\_BITRATE:** set limitation of MUX bitrate

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x630 – HALREG\_AUXDATA\_CNTL:** use in BML async mode

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000001 | AUXDATA\_EN\_STOP |
| 2~31 |  | Reserved |  |

**Description**

AUXDATA\_EN\_STOP: if you use BML async mode, you need to write this flag in HALREG, and update BML stream.

**0x631 - HALREG\_AUXDATA\_STATUS:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | R | 0x00000000 | AUXDATA\_IDLE |
| 1 | R | 0x00000001 | AUXDATA\_ASYNC |
| 2 | R | 0x00000002 | AUXDATA\_SYNC |
| 3~31 |  | Reserved | - |

**0x632 - HALREG\_AUXDATA\_PACHETNUMS:** BML stream packet numbers

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 |  | Reserved |  |

**0x2000 - HALREG\_MUXPSI\_MODE:** Produce mode of PSI

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | MUX\_PURE |
| 3~31 |  | Reserved |  |

**Description**

MUX\_PURE: set PSI mode as PURE mode, VATEK provide PURE mode, user can set PSI table create by themselves.

## 5. PSI Register

### 5.1 Playload Buffer Register

**0x2100 - HALRANGE\_PLAYLOAD\_START:** register of register PSI/SI table start tag, it’s start at 0x2100.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x3000 - HALRANGE\_PLAYLOAD\_END:** register of register PSI/SI table end tag, it’s end at 0x3000

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

### 5.2 PSI Pure Mode

Please follow [appendix A](#_A._Register_PSI/SI)

**0x00 - HALOF\_RAWPSI\_TAG:** start and end tag in PSI PURE mode, you need to use start tag when writing new PSI table, and use end tag after finishing table.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W | 0xFF070600 | RAWPSI\_EN\_TAG |
| W | 0xFF0706FF | RAWPSI\_EN\_ENDTAG |

**0x01 - HALOF\_RAWPSI\_INTERVAL:** PSI Table Interval Time (ms)

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x02 - HALOF\_RAWPSI\_PACKETS:** PSI Table packet size

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x03 – HALOF\_RAWPSI\_DATA:** write PSI table data continuously

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

### 5.3 Private PSI table

Please follow [appendix B](#_B._Insert_PSI/SI)

Private PSI table is the way in PURE mode, it’s only can be inserted table after chip start broadcast, but private PSI provide dynamically modify and insert table.

**0x639 – HALREG\_PRIVATE\_START:** private stream playload start address

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x63A – HALREG\_PRIVATE\_END:** private stream playload end address

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x063B – HALREG\_PRIVATE\_CNTL:** private stream control

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x80000000 | PRIVATE\_EN\_CONTINUE |
| 1 | W | 0x00000001 | PRIVATE\_EN\_TIMES |
| 2~31 | W |  |  |

**Description**

* PRIVATE\_EN\_CONTINUE: when write and read pointer are not equal, user can use this flag to send PSI table to chip.
* PRIVATE\_EN\_TIMES: set PRIVATE\_EN\_TIMES can insert table one time after broadcast start.

**0x63C – HALREG\_PRIVATE\_WPTR:** Private stream write pointer (update by user)

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x63D – HALREG\_PRIVATE\_RPTR:** private stream read pointer (update by hardware)

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

## 6. Modulator Register

### 6.1 Modulator Related Settings

**0x601 - HALREG\_BROADCAST\_OUTPUT:** Broadcast Output Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000003 | RUNMODE\_BROADCAST |
| 1~31 |  | Reserved | -- |

**0x680 - HALREG\_MOD\_MOD:** Modulation Standard Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~3 | W | 0x00000000 | MOD\_DVB\_T |
| W | 0x00000001 | MOD\_J83A |
| W | 0x00000002 | MOD\_ATSC |
| W | 0x00000003 | MOD\_J83B |
| W | 0x00000004 | MOD\_DTMB |
| W | 0x00000005 | MOD\_ISDB\_T |
| W | 0x00000006 | MOD\_J83C |
| W | 0x00000007 | MOD\_DVB\_T2 |
| 4~31 |  | Reserved |  |

**0x681 - HALREG\_MOD\_IFMODE:** Modulation Switch Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000001 | IFMODE\_DISABLE |
| W | 0x00000003 | IFMODE\_IQ\_OFFSET |
| 2~31 |  | Reserved |  |

**Description**

IFMODE\_IQ\_OFFSET: If you want to use ISDB-T modulator type, you should use IFMODE\_IQ\_OFFSET function. VATEK provide baseband offset function, you can set offset value

**0x682 - HALREG\_MOD\_IFFREQ:** baseband offset setting register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
|  | W |  |  |

**Description**

VATEK provide baseband offset function, you can set offset value when you use IFMODE\_IQ\_OFFSET function, it’s usually use in ISDB-T modulator type.

**0x683 - HALREG\_MOD\_DACGAIN:** DAC gain setting register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | DACGAIN\_DEFAULT |
| 1~31 | W |  |  |

**Description**

VATEK provide the default DACGAIN value, but user also can modify DACGAIN value by using this HAL register.

**0x684 - HALREG\_MOD\_BW\_SB:** Modulator bandwidth or symbol rate setting register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 1~31 | W |  |  |

### 6.2 DVB-T Settings

**0x690 - HALREG\_DVB\_T\_CONSTELLATION:** DVB-T Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | DVB\_T\_QPSK |
| 1 | W | 0x00000002 | DVB\_T\_QAM16 |
| 2 | W | 0x00000004 | DVB\_T\_QAM64 |
| 3~31 |  | Reserved | -- |

**0x691 - HALREG\_DVB\_T\_FFT:** DVB-T Carrier Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DVB\_T\_FFT2K |
| W | 0x00000001 | DVB\_T\_FFT8K |
| W | 0x00000002 | DVB\_T\_FFT4K |
| 2~31 |  | Reserved | -- |

**0x692 - HALREG\_DVB\_T\_GUARDINTERVAL:** DVB-T Guard Interval Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DVB\_T\_GI\_1\_32 |
| W | 0x00000001 | DVB\_T\_GI\_1\_16 |
| W | 0x00000002 | DVB\_T\_GI\_1\_8 |
| W | 0x00000003 | DVB\_T\_GI\_1\_4 |
| 2~31 |  | Reserved | -- |

**0x693 - HALREG\_DVB\_T\_CODERATE:** DVB-T Code Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | DVB\_T\_CODERATE\_1\_2 |
| W | 0x00000001 | DVB\_T\_CODERATE\_2\_3 |
| W | 0x00000002 | DVB\_T\_CODERATE\_3\_4 |
| W | 0x00000003 | DVB\_T\_CODERATE\_5\_6 |
| W | 0x00000004 | DVB\_T\_CODERATE\_7\_8 |
| 3~31 |  | Reserved | -- |

### 6.3 DVB-C (J83A) Settings

**0x690 - HALREG\_J83A\_CONSTELLATION:** DVB-C (J83.A) Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | J83A\_QAM16 |
| W | 0x00000001 | J83A\_QAM32 |
| W | 0x00000002 | J83A\_QAM64 |
| W | 0x00000003 | J83A\_QAM128 |
| W | 0x00000004 | J83A\_QAM\_256 |
| 3~31 |  | Reserved | -- |

### 6.4 ATSC (8VSB) Settings

**0x690 - HALREG\_ATSC\_ CONSTELLATION:** ATSC (8VSB) Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | ATSC\_8VSB |
| 1~31 |  | Reserved | -- |

### 6.5 Clear QAM (J83.B) Settings

**0x690 - HALREG\_J83B\_CONSTELLATION:** Clear QAM(J83B) Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000001 | J83B\_QAM64 |
| W | 0x00000003 | J83B\_QAM256 |
| 2~31 |  | Reserved | -- |

### 6.6 DTMB Settings

**0x690 - HALREG\_DTMB\_CONSTELLATION:** DTMB Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | DTMB\_QPSK |
| W | 0x00000001 | DTMB\_QAM16 |
| W | 0x00000002 | DTMB\_QAM64 |
| W | 0x00000004 | DTMB\_QAM32 |
| 3~31 |  | Reserved | -- |

**0x691 - HALREG\_DTMB\_TIME\_INTERLEAVED:** DTMB Time Interleaved Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DTMB\_TI\_DISABLE |
| W | 0x00000001 | Reserved |
| W | 0x00000002 | DTMB\_TI\_240 |
| W | 0x00000003 | DTMB\_TI\_720 |
| 2~31 |  | Reserved | -- |

**0x692 - HALREG\_DTMB\_CODERATE:** DTMB Code Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DTMB\_CODERATE\_0\_4 |
| W | 0x00000001 | DTMB\_CODERATE\_0\_6 |
| W | 0x00000002 | DTMB\_CODERATE\_0\_8 |
| 2~31 |  | Reserved | -- |

**0x693 - HALREG\_DTMB\_CARRIERMODE:** DTMB Carrier Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | DTMB\_CARRIER\_3780 |
| W | 0x00000001 | DTMB\_CARRIER\_1 |
| 1~31 |  | Reserved | -- |

**0x694 - HALREG\_DTMB\_SYNCFRAME:** DTMB Sync Frame Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DTMB\_SYNC\_420 |
| W | 0x00000001 | DTMB\_SYNC\_945 |
| W | 0x00000002 | DTMB\_SYNC\_595 |
| 2~31 |  | Reserved | -- |

### 6.7 ISDB-T Settings

**0x690 - HALREG\_ISDB\_T\_CONSTELLATION:** ISDB-T Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | ISDB\_T\_DQPSK |
| W | 0x00000001 | ISDB\_T\_QPSK |
| W | 0x00000002 | ISDB\_T\_QAM16 |
| W | 0x00000003 | ISDB\_T\_QAM64 |
| 2~31 |  | Reserved | -- |

**0x691 - HALREG\_ISDB\_T\_FFT:** ISDB-T Carrier Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | ISDB\_T\_FFT2K |
| W | 0x00000001 | ISDB\_T\_FFT8K |
| W | 0x00000002 | ISDB\_T\_FFT4K |
| 2~31 |  | Reserved | -- |

**0x692 - HALREG\_ISDB\_T\_GUARDINTERVAL:** ISDB-T Guard Interval Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | ISDB\_T\_GI\_1\_32 |
| W | 0x00000001 | ISDB\_T\_GI\_1\_16 |
| W | 0x00000002 | ISDB\_T\_GI\_1\_8 |
| W | 0x00000003 | ISDB\_T\_GI\_1\_4 |
| 2~31 |  | Reserved | -- |

**0x693 - HALREG\_ISDB\_T\_CODERATE:** ISDB-T Code Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | ISDB\_T\_CODERATE\_1\_2 |
| W | 0x00000001 | ISDB\_T\_CODERATE\_2\_3 |
| W | 0x00000002 | ISDB\_T\_CODERATE\_3\_4 |
| W | 0x00000003 | ISDB\_T\_CODERATE\_5\_6 |
| W | 0x00000004 | ISDB\_T\_CODERATE\_7\_8 |
| 3~31 |  | Reserved | -- |

**0x694 - HALREG\_ISDB\_T\_TIME\_INTERLEAVED:** ISDB-T Time Interleave Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | ISDB\_T\_TI\_DISABLE |
| W | 0x00000001 | ISDB\_T\_TI\_MODE1 |
| W | 0x00000002 | ISDB\_T\_TI\_MODE2 |
| W | 0x00000003 | ISDB\_T\_TI\_MODE3 |
| 2~31 |  | Reserved | -- |

**0x695 - HALREG\_ISDB\_T\_FLAGS:** ISDB-T Flag Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000001 | ISDB\_T\_EN\_AC\_1 |
| W | 0x00000002 | ISDB\_T\_EN\_AC\_2 |
| W | 0x00000004 | ISDB\_T\_EN\_EMERGENCY |
| 2~31 |  | Reserved | -- |

### 6.8 J83.C Settings

**0x690 - HALREG\_J83C\_CONSTELLATION:** J83.C Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | Reserved |  |
| 1 | W | 0x00000002 | J83C\_QAM64 |
| 2 | W | 0x00000004 | J83C\_QAM256 |
| 3~31 |  | Reserved | -- |

### 6.9 DVB-T2 Settings

**0x691 - HALREG\_DVB\_T2\_FLAGS:** DVB-T2 Control Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000001 | T2EN\_EXTEND\_CARRIER\_MODE |
| 1 | W | 0x00000002 | T2EN\_CONSTELLATION\_ROTATION |
| 2 | W | 0x00000004 | T2EN\_INPUT\_TS\_HEM |
| 3 | W | 0x00000008 | T2EN\_DELETE\_NULL\_PACKET |
| 4 | W | 0x00000010 | T2EN\_VBR\_CODING |
| 5 | W | 0x00000020 | T2EN\_TIME\_INTERVAL |
| 6~31 |  | Reserved | -- |

**0x692 - HALREG\_DVB\_T2\_ISSY:** DVB-T2 ISSY Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | T2\_ISSY\_DISABLE |
| W | 0x00000002 | T2\_ISSY\_SHORT |
| W | 0x00000003 | T2\_ISSY\_LONG |
| 2~31 |  | Reserved | -- |

**0x693 - HALREG\_DVB\_T2\_NIT:** DVB-T2 NIT Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | T2\_NTI\_DISABLE |
| 1~31 |  | Reserved | -- |

**0x694 - HALREG\_DVB\_T2\_L1\_CONSTELLATION:** DVB-T2 L1 Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_L1\_BPSK |
| W | 0x00000001 | T2\_L1\_QPSK |
| W | 0x00000002 | T2\_L1\_QAM16 |
| W | 0x00000003 | T2\_L1\_QAM64 |
| 3~31 |  | Reserved | -- |

**0x695 - HALREG\_DVB\_T2\_PLP\_CONSTELLATION:** DVB-T2 PLP Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_PLP\_QPSK |
| W | 0x00000001 | T2\_PLP\_QAM16 |
| W | 0x00000002 | T2\_PLP\_QAM64 |
| W | 0x00000003 | T2\_PLP\_QAM256 |
| 3~31 |  | Reserved | -- |

**0x696 - HALREG\_DVB\_T2\_FFT:** DVB-T2 Carrier Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_FFT\_1K |
| W | 0x00000001 | T2\_FFT\_2K |
| W | 0x00000002 | T2\_FFT\_4K |
| W | 0x00000003 | T2\_FFT\_8K |
| W | 0x00000004 | T2\_FFT\_16K |
| W | 0x00000005 | T2\_FFT\_32K |
| 3~31 |  | Reserved | -- |

**0x697 - HALREG\_DVB\_T2\_CODERATE:** DVB-T2 Code Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_CODERATE\_1\_2 |
| W | 0x00000001 | T2\_CODERATE\_3\_5 |
| W | 0x00000002 | T2\_CODERATE\_2\_3 |
| W | 0x00000003 | T2\_CODERATE\_3\_4 |
| W | 0x00000004 | T2\_CODERATE\_4\_5 |
| W | 0x00000005 | T2\_CODERATE\_5\_6 |
| W | 0x00000006 | T2\_CODERATE\_1\_3 |
| W | 0x00000007 | T2\_CODERATE\_2\_5 |
| 3~31 |  | Reserved | -- |

**0x698 - HALREG\_DVB\_T2\_GUARDINTERVAL:** DVB-T2 Guard Interval Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_GI\_1\_32 |
| W | 0x00000001 | T2\_GI\_1\_16 |
| W | 0x00000002 | T2\_GI\_1\_8 |
| W | 0x00000003 | T2\_GI\_1\_4 |
| W | 0x00000004 | T2\_GI\_1\_128 |
| W | 0x00000005 | T2\_GI\_19\_128 |
| W | 0x00000006 | T2\_GI\_19\_256 |
| 3~31 |  | Reserved | -- |

**0x699 - HALREG\_DVB\_T2\_PILOTPATTERN:** DVB-T2 Pilot Pattern Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_PP\_1 |
| W | 0x00000001 | T2\_PP\_2 |
| W | 0x00000002 | T2\_PP\_3 |
| W | 0x00000003 | T2\_PP\_4 |
| W | 0x00000004 | T2\_PP\_5 |
| W | 0x00000005 | T2\_PP\_6 |
| W | 0x00000006 | T2\_PP\_7 |
| W | 0x00000007 | T2\_PP\_8 |
| 3~31 |  | Reserved | -- |

**0x69A - HALREG\_DVB\_T2\_FECTYPE:** DVB-T2 FEC Frame Length Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | T2\_FEC\_16200 |
| W | 0x00000001 | T2\_FEC\_64800 |
| 1~31 |  | Reserved | -- |

**0x69B - HALREG\_DVB\_T2\_NID:** DVB-T2 NID Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 1~31 |  | Reserved | -- |

**0x69C - HALREG\_DVB\_T2\_SID:** DVB-T2 SID Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 1~31 |  | Reserved | -- |

**0x69D - HALREG\_DVB\_T2\_FECBN:** DVB-T2 FECBN Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 1~31 |  | Reserved | -- |

**0x69E - HALREG\_DVB\_T2\_SBN:** DVB-T2 SBN Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 1~31 |  | Reserved | -- |

## 7. Broadcast Related Registers

### 7.1 General Settings

**0x600 - HALREG\_SERVICE\_BASE\_CNTL:** Broadcast Control Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000001 | BASE\_CMD\_START |
| 1 | W | 0x00000002 | BASE\_CMD\_STOP |
| 2 | W | 0x00000004 | BASE\_CMD\_TEST\_START\_SINE |
| 3 | W | 0x00000008 | BASE\_CMD\_TEST\_START |
| 2~7 |  | Reserved | -- |
| 8 | W | 0x00000100 | BASE\_CMD\_REBOOT |
| 9 | W | 0x00000200 | BASE\_CMD\_REBOOT\_RESCURE |
| 10~11 |  | Reserved |  |
| 12 | W | 0x00001000 | RFMIXER\_CMD\_START |
| 13 | W | 0x00002000 | RFMIXER\_CMD\_STOP |
| 14~31 |  | Reserved | -- |

**Description**

* BASE\_CMD\_START: service start command.
* BASE\_CMD\_STOP: service stop command.
* BASE\_CMD\_TEST\_START\_SINE: use sine wave starting.
* BASE\_CMD\_TEST\_START: test mode start.
* BASE\_CMD\_REBOOT: software reset command using with BASE\_CMD\_REBOOT\_RESCURE, if user want to reset chip by software reset, can using this command without chip fail.
* BASE\_CMD\_REBOOT\_RESCURE: software reset command using with BASE\_CMD\_REBOOT, if user want to reset chip by software reset, can using this command without chip fail.
* RFMIXER\_CMD\_START: RF start command, control by VATek chip.
* RFMIXER\_CMD\_STOP: RF start command, control by VATek chip.

### 7.2 RF Related Settings (For VATEK R2 Control)

**0x1200 - HALREG\_RF\_COM\_STATUS:** R2 Status Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | R | 0x00000001 | RF\_STATUS\_IDLE |
| 1 | R | 0x00000002 | RF\_STATUS\_ACTIVE |
| 2~30 |  | Reserved |  |
| 31 | R | 0x80000000 | RF\_STATUS\_FAIL |

**0x1202 - HALREG\_RF\_COM\_FREQ:** R2 Frequency Register

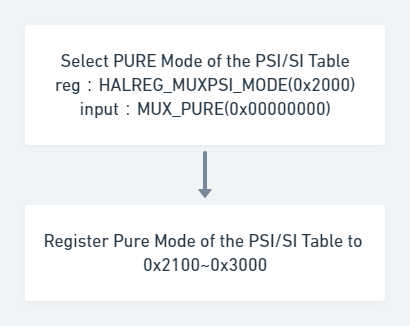
|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W |  | \_\_\_KHz |
| 1~31 |  | Reversed |  |

**Description**

User only need to set RF frequency and write RF start command, RF will start output.

## Appendix

### A. Register PSI/SI table by using PSI PURE mode

Register table during 0x2100 to 0x3000，refer 5.2。

**一張含有 桌 的圖片

自動產生的描述**

PSITABLE\_REGISTER() {

for (i=0; i<Table\_Number; i++) {

RAWPSI\_EN\_TAG

HALOF\_RAWPSI\_INTERVAL

HALOF\_RAWPSI\_PACKETS

HALOF\_RAWPSI\_DATA

}

RAWPSI\_EN\_ENDTAG

}

32

32

32

32\*N

32

Bits

32

32

32

32

32

Syntax

32

32

32

32

32

Table\_Number: number of register PSI/SI table，16 is maximum。

RAWPSI\_EN\_TAG: start tag when registering PSI/SI table。

HALOF\_RAWPSI\_INTERVAL: interval of transport table。

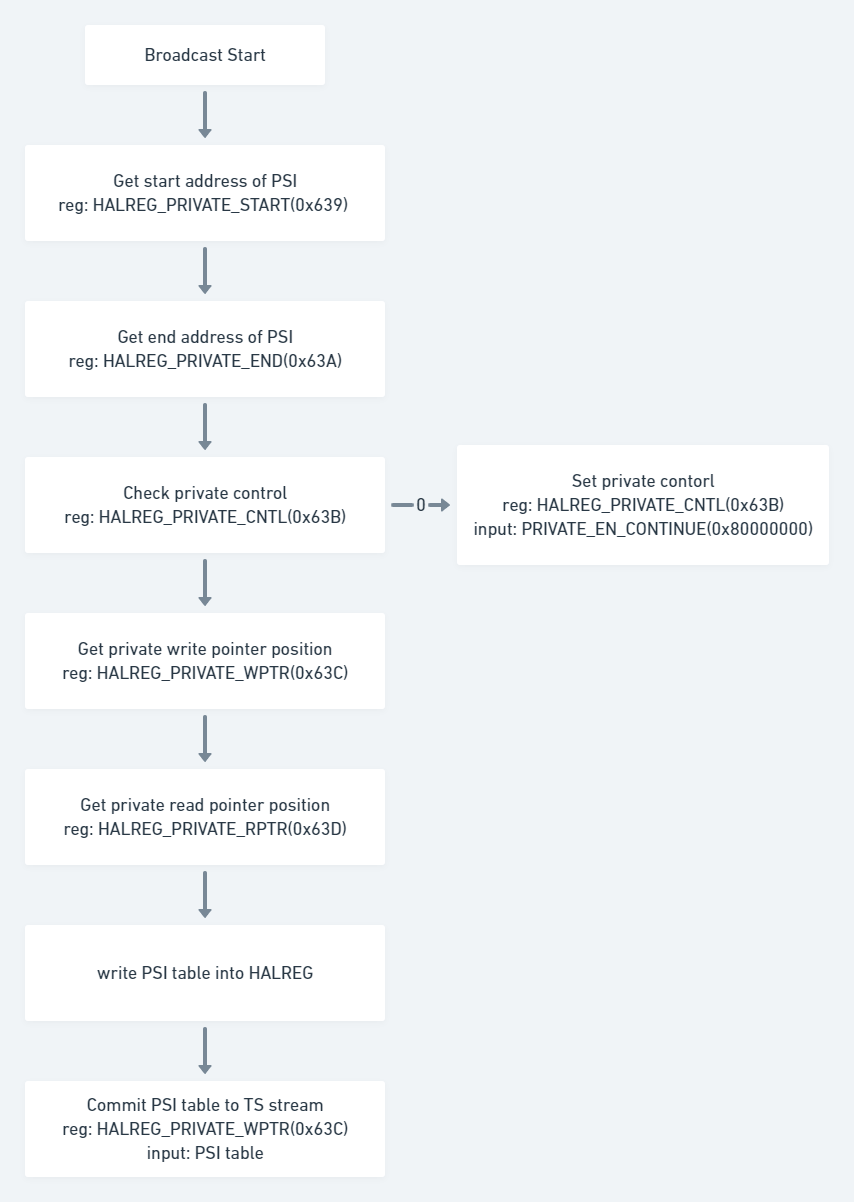
HALOF\_RAWPSI\_PACKETS: packet number of PSI/SI table，each packet max is 188 Bytes。

HALOF\_RAWPSI\_DATA: data of register PSI/SI。

RAWPSI\_EN\_ENDTAG: end tag of register PSI/SI。

### B. Insert PSI/SI table by using PSI PURE mode

Insert table during 0x2100 to 0x3000, refer 5.3



### C. RF start flow (for VATek R2)

